REMARKS

The specification has been amended to make editorial changes to place the application in condition for allowance at the time of the next Official Action.

Claims 1-12 were previously pending in the application. New claims 13-20 are added. Therefore, claims 1-20 are presented for consideration.

Claim 1 is amended and is believed to address the 35 USC §112, second paragraph rejection noted in the Official Action. Specifically, the word "excessively" has been removed to clarify that the claim provides that the reaction layer is either not formed or is suppressed from being formed.

Claims 1, 3 and 5-12 are rejected as unpatentable over VANFLETEREN et al. 6,555,414 in view of SARKHEL et al. 6,010,060 and further in view of KADOMURA 5,540,812. This rejection is respectfully traversed.

Claim 1 provides the step of activating the electrode surfaces of the semiconductor chips which are arranged in opposition to each other.

By way of example, page 8, lines 9-16 of the present application disclose that an organic substance on the surface of solder 4 is removed and activated. This procedure is carried out for each of the semiconductor chips to be laminated.

Accordingly, opposing electrode surfaces (solder 4 in Figure 4A) are both activated and arranged opposite to each other.

As noted in the Official Action, VANFLETEREN et al. in view of SARKHEL et al. fail to disclose the step of activating electrode surfaces of the semiconductor chip (and the substrate).

KADOMURA is offered in an attempt to overcome this shortcoming. Specifically, KADOMURA is offered for the teaching of an activating step carried out to remove an organic substance. Column 2, lines 26-40 of KADOMURA are cited as providing this teaching. However, this teaching is related to the problems of after-corrosion that occurs when etching a layer of aluminum-based material as part of an intermediate step of forming a semiconductor chip. KADOMURA neither teaches or suggests that the activating step is carried out on an external electrode surface of a semiconductor chip or that the activating step is performed on two opposing surfaces that will be bonded to each other in a subsequent step.

MPEP §2143.01 states that "obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. The test for an implicit showing is what the combined

teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 13, 1317 (Fed. Cir. 2000).

KADOMURA is not faced with the same problem to be solved in the present application. Specifically, the present inventors are faced with the problem of keeping electrodes connected without heating so that successive heating steps are not required which increase the size of the reaction layer. Compare the size of the reaction layer in Figure 3C when two chips are combined with the reaction layer in Figure 3D after two heating steps.

KADOMURA faces the problem of corrosion during etching. One of ordinary skill in the art based on the problem to be solved in the teachings of KADOMURA would not combine KADOMURA with VANFLETEREN et al. and SARKHEL et al. to render obvious claim 1 of the present invention.

In addition, even if KADOMURA were combined with VANFLETEREN et al. and SARKHEL et al., there is no teaching in the references that two opposing surfaces should be activated. VANFLETEREN et al. in conjunction with Figures 4A-4F teach applying a conductive adhesive 6 to a single surface, i.e. the surface of electrical contact pads 2a of substrate 3. SARKHEL et al. teach a single solder connection between bumps. Accordingly,

there is neither motivation to combine the references as proposed nor would the proposed combination of references teach each of the recited steps of claim 1. Therefore, *prima facie* obviousness has not been established and reconsideration and withdrawal of the rejection are respectfully requested.

Claims 3 and 5-12 depend from claim 1 and further define the invention and are also believed patentable over the proposed combination of references.

Claim 2 is rejected as unpatentable over VANFLETEREN et al. in view of SARKHEL et al. and KADOMURA and further in view of TANAKA 5,889,326. This rejection is respectfully traversed.

TANAKA is only cited for the teaching of applying a supersonic wave in addition to pressing in a bonding step. TANAKA does not teach or suggest what is recited in claim 1. As set forth above, VANFLETEREN et al. in view of SARKHEL et al. and KADOMURA do not teach or suggest what is recited in claim 1. Since claim 2 depends from claim 1 and further defines the invention, the proposed combination of references would not render obvious claim 2.

Claim 4 is rejected as unpatentable over VANFLETEREN et al. and SARKHEL et al. in view of KADOMURA and further in view of SENDA et al. 5,576,053. This rejection is respectfully traversed.

SENDA et al. is only cited for the teaching of forming an electrode by electroless plating. SENDA et al. do not teach or suggest what is recited in claim 1. As set forth above, VANFLETEREN et al. and SARKHEL et al. in view of KADOMURA do not teach or suggest what is recited in claim 1. Since claim 4 depends from claim 1 and further defines the invention, the combination of references would not render obvious claim 4.

By way of further explanation, according to the present invention, it is possible to sequentially mount the semiconductor chips without a heating treatment. As a result, the semiconductor chips can be mounted upon the contemporary connection without the compound (the reaction layer) being formed. Thereafter, by entirely heating the semiconductor chips, the reaction layers can be uniformly formed for the respective connection portions of the semiconductor chips.

Moreover, since the heating treatment is unnecessary upon mounting the semiconductor chips, it is possible to mount the semiconductor chips with the high accuracy without being affected by the ambient temperature.

In VANFLETEREN et al., the temporary connection is carried out for the semiconductor chips by the resin connection. After the temporary connection, the reflow is carried out so as to perform the welding connection for the semiconductor chips.

Thus, the heating treatment is carried out until the curing temperature of the epoxy resin in order to cure the resin. As a consequence, upon mounting, the compound (the reaction layer) is formed at the connection portions of the semiconductor chips by this heating treatment.

Further, it is difficult to achieve the high positioning accuracy upon mounting because of the above-mentioned heating treatment.

Furthermore, in VANFLETEREN et al., the semiconductor chips are arranged in the two-dimensional form, and therefore, the thermal hysteresis does not give any affect for the adjacent semiconductor chips upon mounting. Consequently, it is unnecessary to take the accumulation of the thermal hysteresis for the connection portion into consideration.

By contrast, according to the present invention, the semiconductor chips are mounted in the three-dimensional form (the vertical direction). Therefore, if it is assumed that the semiconductor chips are sequentially mounted with the heat treatment, the previously mounted chip will be inevitably subjected to the heat treatment again via the thermal conduction of the semiconductor chip. Thus, according to the present invention, it is necessary to take the accumulation of the thermal hysteresis for the connection portion into consideration because of the three-dimensional form. The proposed combination

of references does not address this feature and thus their combination would not render obvious claim 1.

New claim 14 provides the step of placing solder on opposing bumps of adjacent semiconductor chips, activating a surface of the solder and directly contacting at least two opposing bumps of adjacent semiconductor chips with each other and pressing the adjacent semiconductor chips together to bond them without heating. New claim 16 provides that the step of pressing comprises bonding by interatomic force. New claim 19 provides the step of directly contacting at least two opposing bumps of adjacent semiconductor chips with each other and pressing the adjacent semiconductor chips together to bond them without heating. The proposed combination of references does not disclose or suggest these steps. Support for the new claims can be found on page 8, lines 9-25 and page 10, lines 3-25, for example.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R.§1.17.

Respectfully submitted,

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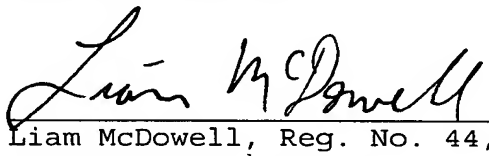

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